



U.S. Patent Application Serial No. 09/855,590

ABSTRACT OF THE DISCLOSURE:

In a semiconductor device having a multiple layer wiring structure, a wiring method, a wiring device, and a recording medium, by optimizing the placement of SVIA, it is possible, for an intersection portion where a lower metal wiring layer having a width $W1$ and an upper metal wiring layer having a width $W4$ intersect with the intermediate metal layers sandwiched in between, to delete one row in the X direction and two rows in the Y direction for a total of nine SVIAs, when five SVIAs are arranged at the pitch PX in the X direction (i.e., in the transverse direction of the upper metal wiring layer) and three SVIAs are arranged at the pitch PY in the Y direction (i.e., in the transverse direction of the lower metal wiring layer) for a total of fifteen SVIAs. As a result, it is possible to secure one wiring track through which wiring is able to pass from among the three wiring tracks in the X direction and two wiring tracks through which wiring is able to pass from among the five wiring tracks in the Y direction.

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